GPS Engine Module

TEK103H-6 GPS Receiver

REV 1.10

CONTENTS

1. SYSTEM DESCRIPTION

1.1 General Description

A complete GPS receiver is implemented on the TEK103H-6 module. The module includes the following features:

- 25.4x25.4mm form factor
- Input for Active GPS antenna bias supply
- 16.3676MHz TCXO
- GPS radio based on uN8021 RF chip
- GPS base-band processor based on uN8031 chip
- Dual UART (3V CMOS levels) for serial data
- SPI-interface (option)
- 16-bit GPIO interface
- 32768Hz RTC
- 16Mbit FLASH memory (1024k x 16bit)

The receiver needs only the following external inputs:

- Regulated 2.7 ~ 3.3V supply
- Active GPS antenna bias supply (if needed)
- External reset input
- GPS Antenna signal (passive or active antenna)

1.2 Physical specification

- Size: 25.4 x 25.4 x 3.0 mm
- Operating Temperature: -40 ºC to +85 ºC
- Operating Humidity: 0% to 95% RH, non condensing
- Vibration: 4 G

1.3 Technical specification

- Receiver: L1, C/A code
- Channels: 12
- Update rate: 1 Hz or user configurable
- AGC Range: 0…+32dB external gain
- Power supply: 2.7 ~ 3.3V, regulated power
- Recommended Supply: 3.0 V
- TTFF: Hot Start: 8.6 sec typ
  Warm Start: 38 sec typ
  Cold Start: 53 sec typ
- Sensitivity: - 138 dBm (Acquisition)
  - 150.5 dBm (Navigation)
  - 152 dBm (Tracking)
- Power Consumption: *Navigating:* 130mW @ 2.7V ave.
  Idle mode(Navigation stopped): 22mW @2.7V typ.
  Sleep mode: 120μW @ 2.7V typ.
  RTC Back-Up mode: 1.5 uA max
- Protocols: NMEA-0183 V3.0, proprietary iTALK binary protocol

1.4 Block diagram

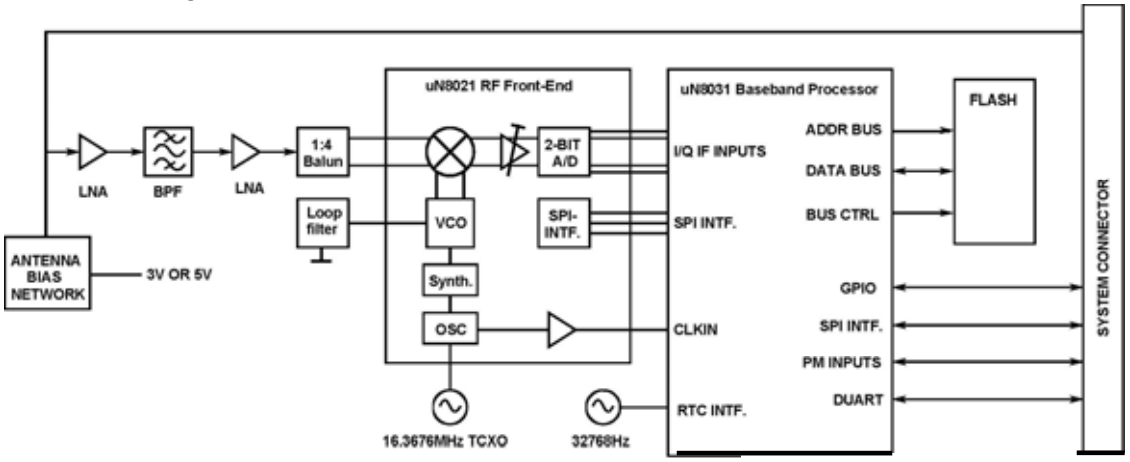


Figure 1 Block diagram of TEK103H-6 GPS receiver

2. MECHANICAL SPECIFICATION Pictures

2.1 Pictures

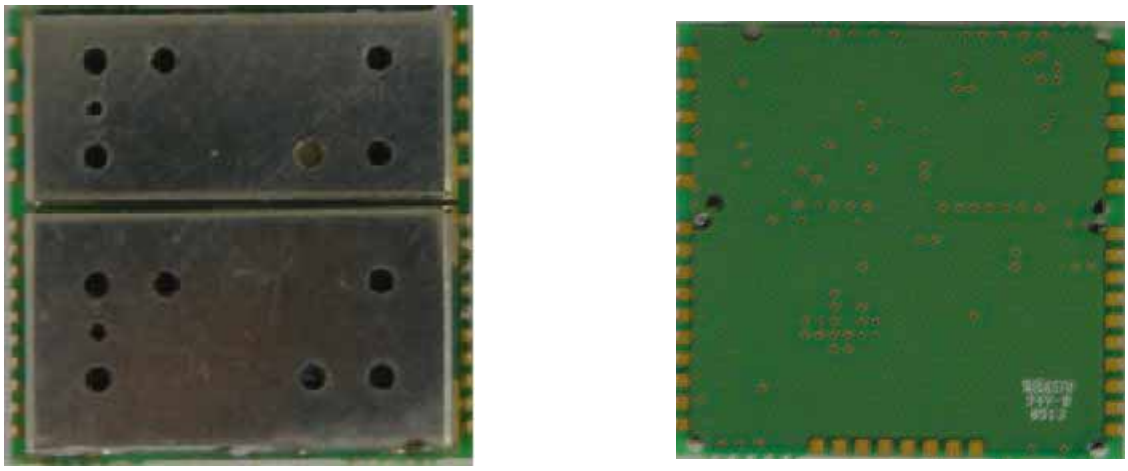


Figure 2 TEK103H-6 modules w/ shield

Figure 3 TEK103H-6, Top view w/o shield

2.2 TEK103H-6 Pin Configurations

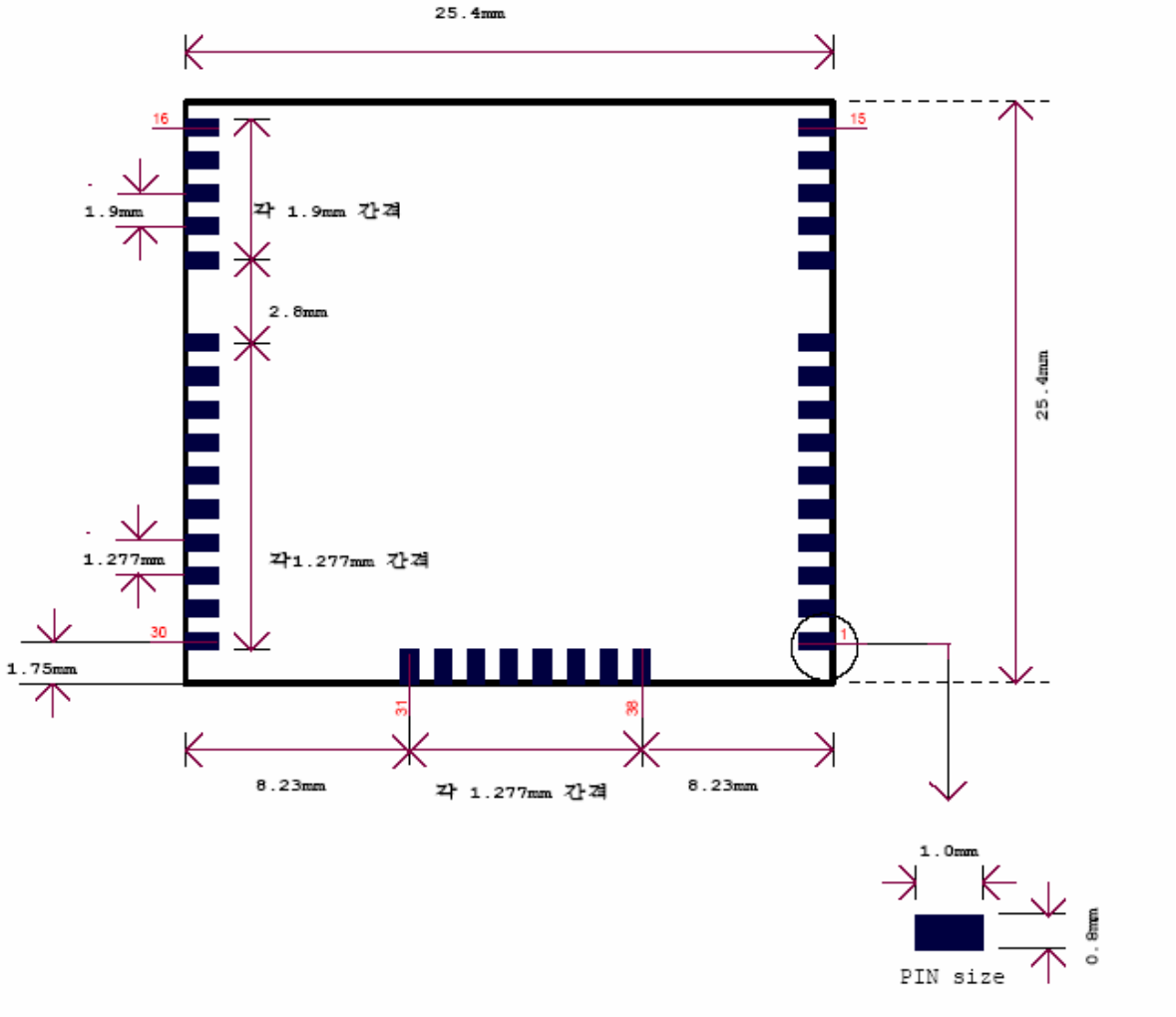


Figure 4 Pin Configuration

3. EXTERNAL INTERFACES

3.1 System connector

- RF Input A
- GPIO[0..15] GPIO-lines I/O
- UART ports PORT0 and PORT1 UART ports I/O
- XRESET External reset (active low) I
- Supply voltage S
- V_ANTENNA External antenna bias S

Table 1 System connector

TEK103H-6			
	PIN	**I/O**	**Note**
1	VCC	Input	Supply Voltage
2	GND	Input	Power and signal ground
3	GPIO15	Input	Boot Mode Select (2)
4	RXD0	Input	UART Port 0, Receive Data (3)
5	TXD0	Output	UART Port 0, Transmit Data
6	TXD1	Output	UART Port 1, Transmit Data
7	RXD1	Input	UART Port 1, Receive Data (3)
8	GPIO3	I/O	General Purpose I/O (1)
9	RF_ON	Output	High if VCC_RF is on
10	GND		Power and signal ground
11	GND		Power and signal ground
12	GND		Power and signal ground
13	GND		Power and signal ground
14	GND		Power and signal ground
15	GND		Power and signal ground
16	GND		Power and signal ground
17	RF	Input	RF input, 50 ohm
18	GND		Power and signal ground
19	V_ANTENNA	Input	Leave unconnected if not used
20	VCC_RF	Output	Can be used as power supply for an active antenna
21	V_Bat	Input	Backup voltage supply for RTC
22	XRESET	Input	Active low reset (4)
23	GPIO10	I/O	General Purpose I/O (1)
24	GPIO6	I/O	General Purpose I/O (1)
25	GPIO5	I/O	General Purpose I/O (1)
26	GPIO7	I/O	General Purpose I/O (1)
27	GPIO0	I/O	General Purpose I/O (1)
28	GPIO1	I/O	General Purpose I/O (1)
29	GPIO4	I/O	General Purpose I/O (1)
30	GND		Power and signal ground
31	GPIO12	I/O	General Purpose I/O (1) SPI Interface Data In (Option) (5)
32	GPIO13	I/O	LNA control (0:LNA ON, 1:LNA OFF)
33	GPIO14	I/O	General Purpose I/O (1)
34	NC		NC
35	GPIO2	I/O	General Purpose I/O (1)

36	GPIO9	I/O	RTC Chip Control (SDA)
37	GPIO8	I/O	RTC Chip Control (SCL)
38	GPIO11	I/O	Wake-UP (1)

Notes:

(1): The base-band processor uN8031 includes a keeper so that no external pull down or pull up resistor is needed. VIH min = 0.7 x VBB, VIL max = 0.3 x VBB. When the GPIO is configured as an input (e.g. External Wake-up GPIO11), the drive impedance should be less than 10kohm in order to change the state.

(2): TEK103H-6 module contains internal 100k pull up resistor to VCC. VIH min = 0.7 x VCC, VIL max = 0.3 x VCC. The base-band processor uN8031 includes also a keeper and the drive impedance should be less than 10kohm in order to change the state.

(3): The base-band processor uN8031 includes an internal 100k pull up resistor to VCC (no keeper). VIH min = 0.7 x VCC, VIL max = 0.3 x VCC.

(4): TEK103H-6 module contains internal 10k pull up resistor to VCC. VIH min = 0.7 x VCC, VIL max = 0.3 x VCC.

(5): The base-band processor uN8031 includes an internal 10k pull up resistor to VCC (no keeper). VIH min = 0.7 x VCC, VIL max = 0.3 x VCC.

Some of the inputs of the uN8031 include a pull-up or a pull-down resistor or a keeper; therefore external resistors to the TEK103H-6 are not required. Unused pins can be left unconnected.

3.2 Reset

NOTE

TEK103H-6 requires an external Power-On-Reset (POR) circuit which provides a reset pulse at XRESET-pin after the supply voltages are connected. The reset pulse should be active (low state) at least 100ms after power-up.

3.3 UART interface

Two asynchronous UART ports are available for serial interfacing. The baud rates are fully programmable.

The data format is however fixed: x, N, 8, 1, i.e. x baud, No parity, eight data bits and 1 stop bit. No other data formats are supported. LSB is sent first. CMOS signal levels are used.

Parity: N
Data Bits: 8
Stop bits: 1

Figure 7 UART Data format.

The UART ports are named PORT0 and PORT1. PORT0 is used e.g. for booting. PORT1 can be utilized for the emulator or NMEA interface.

3.4 GPIO interface

A 16-bit GPIO port is available for external interfaces. Each of the GPIO-lines can be programmed for generating interrupts. Two of the GPIO-lines (GPIO14 and GPIO15) are reserved for Boot Mode Select as described below. And GPIO8 and GPIO9 are reserved for external RTC-Chip control.

Table 2 Boot mode select

GPIO15	GPIO14	Boot Mode
0	x	Boot from flash

The TEK103H-6 is configured for booting from Flash memory as a default. This is achieved with the internal pull-up resistors R12 and R13 at GPIO14&15. Other boot modes can be selected with external drive at the system connector (i.e. in Evaluation Kit, or by external host) at GPIO14&15.

One of the GPIO-lines (GPIO13) is reserved for active power control of the internal LNA and it can be also used for controlling external LNA. Also GPIO12 is reserved internally for controlling the flash memory.

GPIO11 is reserved for external Wake-up after setting TEK103H-6 to sleep state. The GPIO11 detects a transition from state 1->0 or from 0->1 as a Wake-up command.

NOTE

When the GPIO is configured as an input (e.g. GPIO11, 14 and 15), the keeper on the base-band processor uN8031 needs less than 10kohm drive impedance in order to change the input state.

3.5 RF-interface

An external GPS antenna (active or passive) can be connected to the TEK103H-6 using the RF-input line. A 50 ohm PCB stripline is needed on the motherboard, see figure below for example layout.

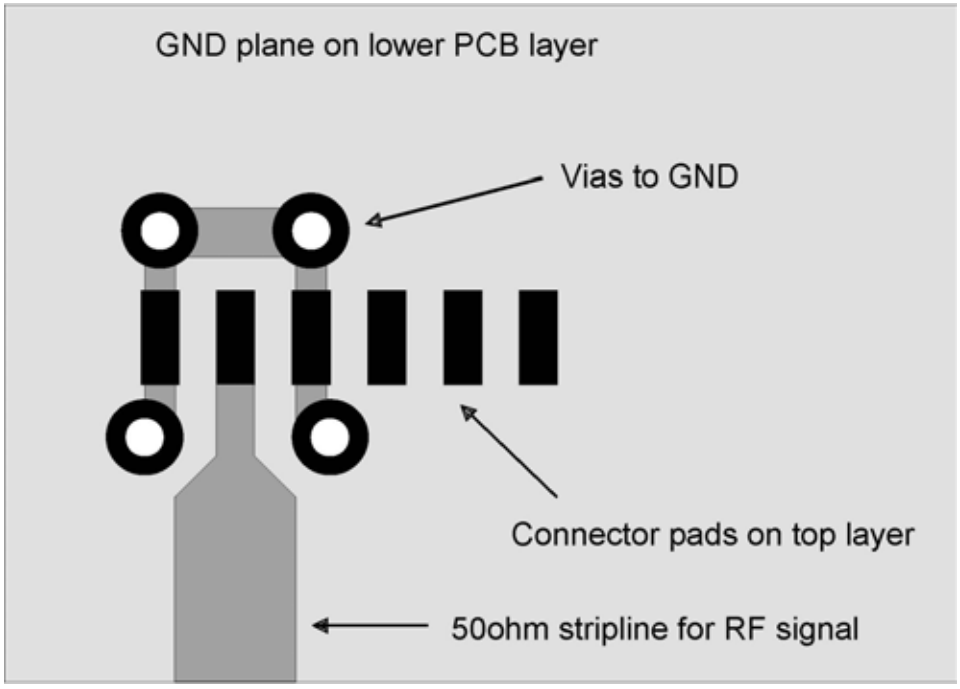


Figure 8 Example of RF interface layout on customer PCB

The width of the 50ohm stripline is dependent of the PCB material and thickness. On FR4 material the width [W] (at 1.5GHz) is roughly 2 times the thickness [H] of the PCB. If the PCB thickness is for example 0.8mm then the width of the stripline should be 1.6mm and so on.

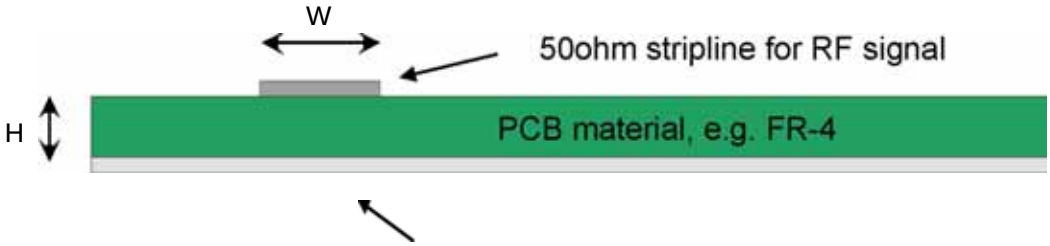


Figure 9 Stripline widths versus PCB thickness

The antenna bias for an external active antenna can be provided through the V_ANTENNA input found on system connector. The V_ANTENNA voltage should be chosen according to the antenna to be used.

NOTE

Maximum supply current for V_ANTENNA should be externally limited to 100mA.

The internal bias network is formed by a stripline, ferrite coil and coupling capacitor, which are used for passing the antenna bias voltage to the RF-input.

3.6 Interfacing considerations

The following recommendations should be taken into account when interfacing to the TEK103H-6 GPS receiver:

- The TEK103H-6 can be used with passive antennas if the cable loss is below 1 dB. Otherwise an active antenna is needed to compensate for the cable loss. Net gain from the active antenna prior TEK103H-6 should be between 6 and 32 dB.

- Use a solid GND plane under the TEK103H-6 module to reduce LO-leakage at 1575 MHz, especially when the GPS antenna is close (<0.2 m) to the module.

- AGC range is 32 dB, which means that for TEK103H-6 module the external gain at 1575 MHz should not exceed 32 dB

- Due to the high external gain strong out-of-band signals may block the front-end. Blocking level is about –2 dBm at the RF input @ S/N degradation 3 dB.

The receiver has a zero-IF topology. If two receivers are connected to the same antenna, the local oscillator leakage may cause blocking. Use a power combiner/splitter that gives at least 20 dB isolation between ports.

4. APPLICATION NOTES FOR TEK103H-6

4.1 External Interfaces

This section describes a recommended interface for the TEK103H-6 receiver.

The minimum set of external interfaces is:

- Power supply
- RF input
- External Reset

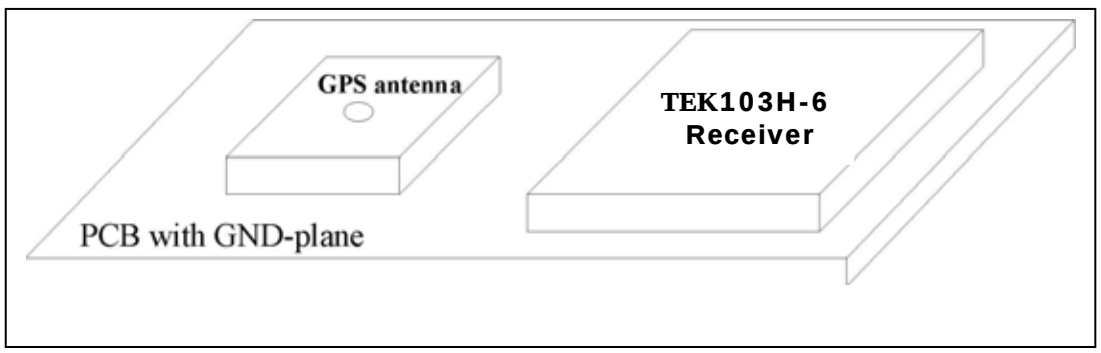
Additionally there are some useful interfaces:

- Boot Mode Select using GPIO15 (dedicated GPIO pin)
- Control of external antenna bias through GPIO13 (dedicated GPIO pin)
- External Wake-up control using GPIO11 (dedicated GPIO pin)

Rest of the I/O is also available for customer applications.

4.2 Antenna issues

The TEK103H-6 GPS receiver can be used with a passive antenna. One typical application is shown below where the GPS antenna and the receiver are adjacent on the same side of the PCB.



In case a patch antenna element is used the user must take into account a few factors that affect antenna performance:

- Size of patch element: smaller elements tend to give lower signal levels due to reduced radiation efficiency.
- Size of GND plane under the patch element: smaller than 70mm GND plane reduces antenna directivity and signal levels.
- Avoid unsymmetrical GND plane: polarization characteristics declines causing polarization miss match loss (reduction in signal levels) and reduction in multi path mitigation (navigation accuracy).

These all issues affect the radiation pattern and the resonance frequency of the antenna. The antenna selection and design is a very critical issue and must be reviewed case-by-case.

Note also that the enclosure material (e.g. plastic cover) also affect the resonance frequency in such a way that plastic material close to the antenna element move the resonance frequency downwards. This must be taken also into consideration when specifying the antenna resonance frequency.

4.3 Application Circuit